IN THE CLAIMS

This listing of claims replaces all prior listings:

1. (withdrawn) An insulated gate field effect transistor having a gate electrode on a substrate with a gate insulating film interposed between said substrate and said gate electrode, and having a source region and a drain region formed in said substrate on both sides of said gate electrode, said insulated gate field effect transistor comprising:

a first diffusion layer of a first conduction type formed in said substrate at a position deeper than said source region and said drain region; and

a second diffusion layer of the first conduction type having a higher concentration than said first diffusion layer and formed in said substrate at a position deeper than said first diffusion layer.

2. (withdrawn) An insulated gate field effect transistor as claimed in claim 1,

wherein a diffusion layer of a second conduction type is formed between said source region and said drain region in said substrate with a region of said substrate left on a side of said gate electrode.

3. (withdrawn) An insulated gate field effect transistor as claimed in claim 2,

wherein said first conduction type is a P type, and said second conduction type is an N type.

4. (canceled).

5. (canceled).

6. (withdrawn) An image pickup device, wherein a part or all of insulated gate field effect transistors forming an output circuit in the image pickup device and formed in a substrate comprise:

a first diffusion layer of a first conduction type formed in said substrate at a position deeper than each source region and each drain region of said insulated gate field effect transistors; and

a second diffusion layer of the first conduction type having a higher concentration than said first diffusion layer and formed in said substrate at a position deeper than said first diffusion layer.

7. (previously presented) A method of manufacturing an image pickup device having at least one insulated gate field effect transistor in an output circuit of the image pickup device and that is formed in a substrate, said method comprising the steps of:

forming, prior to forming said insulated gate field effect transistor, a first diffusion layer of a first conduction type in said substrate beneath where said insulated gate field effect transistor is to be formed, at a position deeper than a region where a source region and a drain region of said insulated gate field effect transistor are to be formed, the first diffusion layer underlying an entire area of said source region and an entire area of said drain region and entirely separated from said source region and said drain region; and

forming, prior to forming said insulated gate field effect transistor, a second diffusion layer of the first conduction type having a higher concentration than said first diffusion layer in said substrate at a position deeper than said first diffusion layer, the second diffusion layer being entirely separated from said first diffusion layer by an intervening layer having a conduction type that is different than the first conduction type.